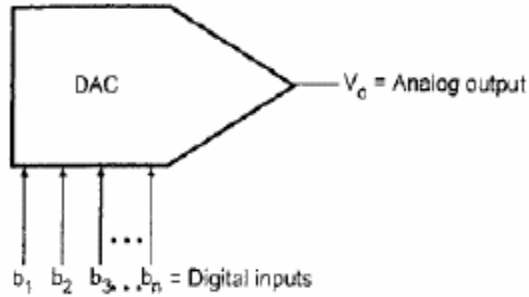
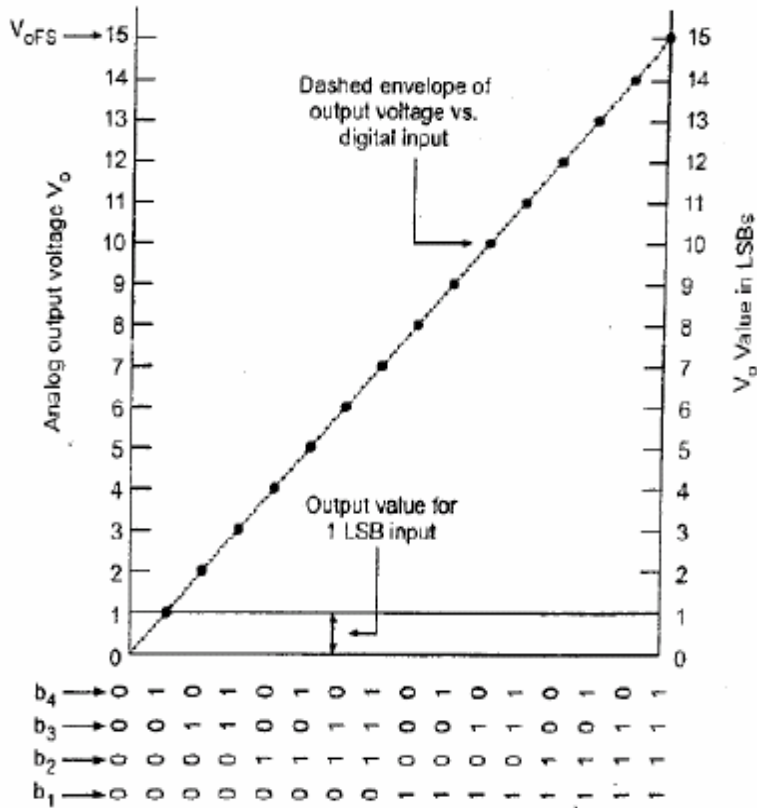


Digital to Analog Converters

A DAC (Digital to Analog Converter) accepts an n-bit input word $b_1, b_2, b_3, \dots, b_n$ in binary and produce an analog signal proportional to it. Figure below shows the circuit symbol and input-output characteristics of a 4-bit DAC.



Each digital input requires an electrical signal representing either logic 1 or a logic 0. The b_n is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB. Figure shows analog output voltage V_o is plotted against all 16 possible digital input words.



Performance Parameters of DAC

The various performance parameters of DAC are,

Resolution

Resolution is defined in two ways.

* Resolution is the number of different analog output values that can be provided by a DAC. For an n-bit DAC,

$$\text{resolution} = 2^n$$

* Resolution is also defined as the ratio of a change in output voltage resulting from a change of 1 LSB at the digital inputs. For an n-bit DAC it can be given as

$$\text{resolution} = \frac{V_{\text{oFS}}}{2^n - 1}$$

Where, V_{oFS} = Full scale output voltage

From equation (1), we can say that, the resolution can be determined by the number of bits in the input binary word. For an 8-bit DAC resolution can be given as

$$\begin{aligned}\text{Resolution} &= 2^n = 2^8 \\ &= 256\end{aligned}$$

If the full scale output voltage is 10.2 V then by second definition the resolution for an 8-bit DAC can be given as

$$\begin{aligned}\text{Resolution} &= \frac{V_{\text{oFS}}}{2^n - 1} = \frac{10.2}{2^8 - 1} = \frac{10.2}{255} \\ &= 40 \text{ mV/1 SB}\end{aligned}$$

Therefore, we can say that an input change of 1 LSB causes the output to change by 40 mV.

From the resolution, we can obtain the input-output equation for a DAC.

Thus, $V_o = \text{resolution} \times D$, Where, D = decimal value of the digital input, and V_n = output voltage. The resolution takes care of changes in the input.

Accuracy

It is a comparison of actual output voltage with expected output. It is expressed in percentage.

Ideally, the accuracy of DAC should be, at worst, $\pm \frac{1}{2}$ of its LSB. If the full scale output voltage is 10.2 V then for a 8-bit DAC accuracy can be given as

$$\begin{aligned}\text{Accuracy} &= \frac{V_{\text{oFS}}}{(2^n - 1)2} \\ &= \frac{10.2}{255 \times 2} = 20 \text{ mV}\end{aligned}$$

Conversion Time

It is a time required for conversion of analog signal into its digital equivalent. It is also called setting time. It depends on the response time of the switches and the output of the amplifier.

Monotonicity

A converter is said to have good monotonicity, if it does not miss any step backward when stepped through its entire range by a counter.

Stability

The performance of converter changes with temperature, age and power supply variations. So all the relevant parameters such as offset, gain, linearity error and monotonicity must be specified over the full temperature and power supply ranges. These parameters represent the stability of the converter.

An 8 bit DAC has an output voltage range of 0 – 2.55 V. Define its resolution in two ways.

Solution :

For the given DAC,

$$n = \text{number of bits} = 8$$

$$\text{i) resolution} = 2^n = 2^8 = 256$$

i.e. the output voltage can have 256 different values including zero.

$$\begin{aligned}\text{ii) } V_{\text{oFS}} &= \text{Full scale output voltage} \\ &= 2.55 \text{ V}\end{aligned}$$

$$\begin{aligned}\text{resolution} &= \frac{V_{\text{oFS}}}{2^n - 1} = \frac{2.55}{2^8 - 1} \\ &= \frac{10 \text{ mV}}{1 \text{ LSB}}\end{aligned}$$

Thus an input change of 1 LSB causes the output to change by 10 mV

The digital input for a 4-bit DAC is 0110. Calculate its final output voltage.

Solution : For given DAC,

$$n = 4$$

$$\therefore V_{\text{oFS}} = 15 \text{ V}$$

$$\therefore \text{resolution} = \frac{V_{\text{oFS}}}{2^n - 1} = \frac{15}{2^4 - 1} = 1 \text{ V/LSB}$$

$$\therefore V_o = \text{resolution} \times D$$

$$\text{Now } D = \text{decimal of } (0110)_2 = 6$$

$$\therefore V_o = 1 \text{ V/LSB} \times 6 = 6 \text{ V}$$

Problem: A 12-bit DAC has a step size of 8 mV. Determine the full scale output voltage and percentage resolution. Also find the output voltage for the input of 010101101101?

$$V_{\text{oFS}} = 8 \text{ mV} \times 2^{12} - 1 = 32.76 \text{ V}$$

$$\% \text{ Resolution} = \frac{8 \text{ mV}}{32.76 \text{ V}} \times 100 = 0.02442\%$$

The output voltage for the input 010101101101 is $= 8 \text{ mV} \times (1389)_{10} = 11.12 \text{ V}$.

Types of D/A Converter

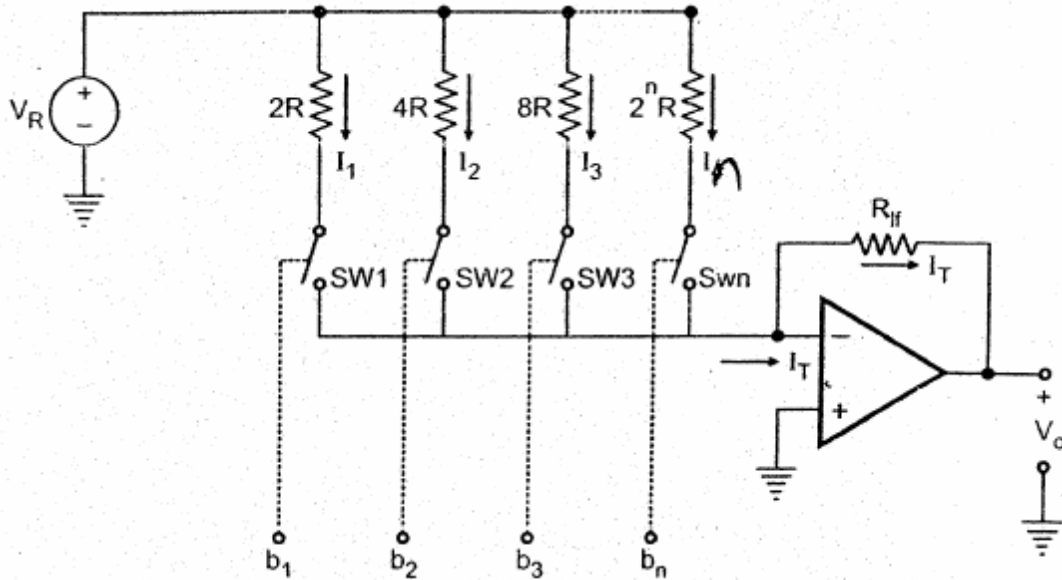
There are mainly two techniques used for analog to digital conversion.

1. Binary weighted resistor D/A converter.
2. R/2R ladder D/A converter

In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called current driven DACs.

Binary Weighted Resistor D/A Converter

The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors $2R, 4R, 8R, \dots, 2^n R$. This circuit arrangement is shown in the figure.



Switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage V_R ; otherwise, it leaves resistor open. Hence,

For ON-switch, $I = \frac{V_R}{R}$ and

For OFF-switch, $I = 0$

Here, operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through R_f . Hence the total current through R_f can be given by

$$I_T = I_1 + I_2 + I_3 + \dots + I_n$$

The output voltage is the voltage across R_f and it is given as

$$\begin{aligned} V_o &= -I_T R_f = (I_1 + I_2 + I_3 + \dots + I_n) R_f \\ &= \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right) R_f \\ &= -\frac{V_R}{R} R_f (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n}) \end{aligned}$$

When $R_f = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

The above equation indicates that the analog output voltage is proportional to the input digital word. The simplicity of the binary weighted DAC is offset by drawbacks associated with it.

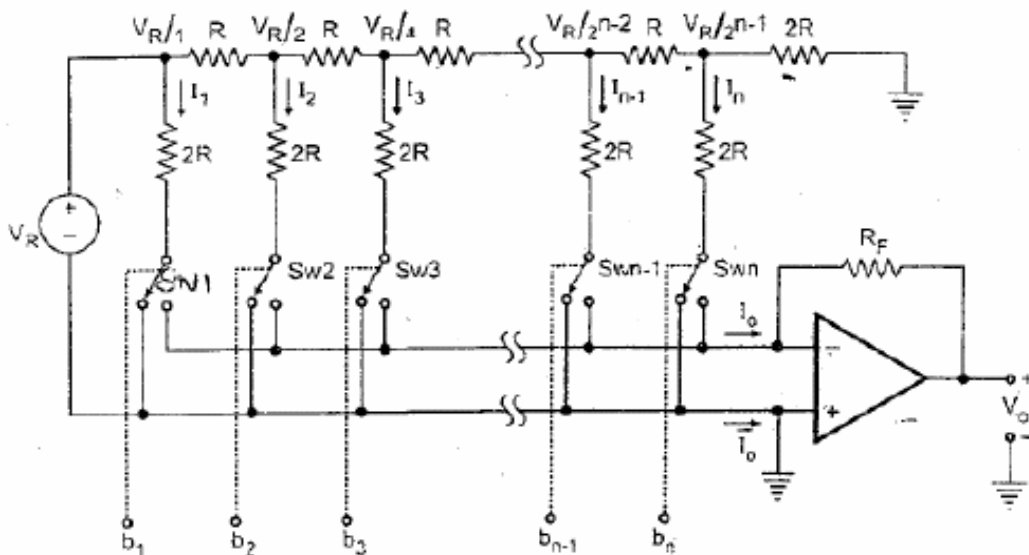
Drawbacks:

1. Wide range of resistor values are required. For 8-bit DAC, the resistors required are $2^1 R$, $2^2 R$, $2^3 R$ and $2^8 R$. Therefore, the largest resistor is 128 times the smallest one.
2. This wide range of resistor values has restrictions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across such a large resistor due to the bias current also affects the accuracy. For smaller values of resistors, the loading effect may occur.
3. The finite resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.

All these drawbacks, especially the requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8-bits.

Inverted R-2R Ladder / Current Mode R-2R Ladder D/A Converter

R/2R ladder D/A converter uses only two resistor values. This avoids resistance spread drawback of binary weighted D/A converter. Fig.4.13 shows R/2R ladder DAC. Like binary weighted resistor DAC, it also uses shunt resistors to generate n binary weighted currents; however it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC. Voltage scaling requires an additional set of voltage dropping series resistances between adjacent nodes, as shown in the figure.



Here, each bit of the binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is at the virtual ground. Since both the positions of switches are at ground potential, the current flowing through resistances is constant and it is independent of switch position. These currents can be given as

$$I_1 = \frac{V_R}{2R}$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^{n-1}}{2R} = \frac{I_1}{2^{n-1}}$$

We know tht, V_o is given as

$$V_o = -I_R R_f$$

$$V_o = R_f (I_1 + I_2 + I_3 + \dots + I_n)$$

$$= R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \dots + b_n \frac{V_R}{2^n R} \right)$$

$$= \frac{V_R R_f}{R} (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

When $R_f = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \dots + b_n 2^{-n})$$

Let us consider 4-bit binary DAC with binary input 1001 and $R_f = R$, as shown in the Fig.

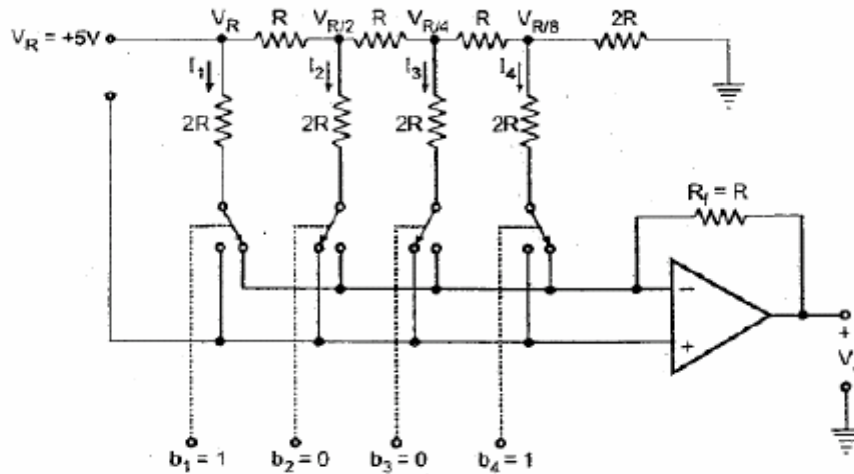


Fig.4.14 Inverted 4-bit R/2R ladder DAC

Here, output voltage is given as

$$\begin{aligned}
 V_o &= V_R (1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4}) \\
 &= -V_R \left(\frac{1}{2} + 0 + 0 + \frac{1}{16} \right) = -0.5625 V_R = 2.8125 \text{ V}
 \end{aligned}$$

The inverting R/2R ladder DAC works on the principle of summing currents and it is also said to operate in the current mode. An important advantage of the current mode is that all ladder node voltages remain constant with changing input codes, thus avoiding any shutdown effects by stray capacitances.

Problem: Suggest the values of resistors and reference voltage if resolution required is 0.5 V for 4 bit R/2R ladder type DAC.

Solution :

$$\text{Resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R} \right) \times R_f$$

Let $V_R = 10 \text{ V}$, $n = 4$ and resolution = 0.5

$$\therefore 0.5 = \frac{1}{2^4} \times \frac{10}{R} \times R_f$$

$$\therefore \frac{R}{R_f} = 1.25$$

Choose $R_f = 10 \text{ k}\Omega$

$$\therefore R = 12.5 \text{ k}\Omega$$

Advantages of R-2R ladder DACs:

1. Easier to build accurately as only two precision metal film resistors are required.
2. Number of bits can be expanded by adding more sections of same R/2R values.
3. In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.